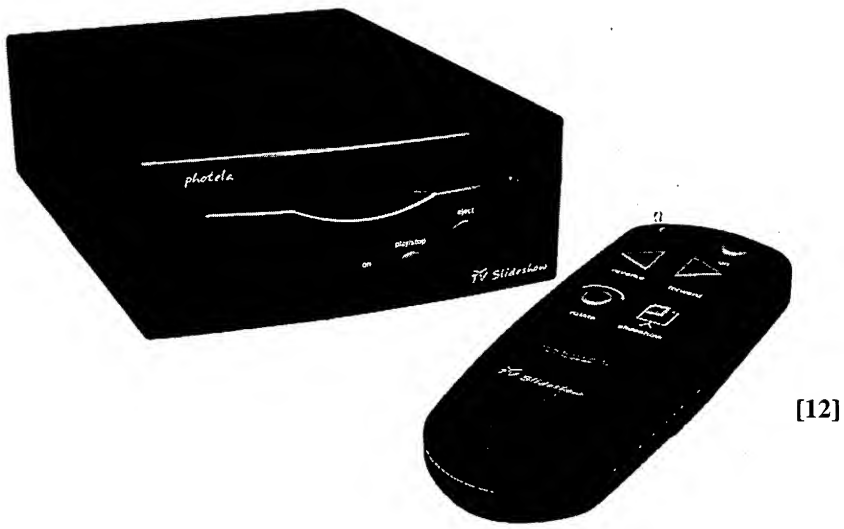
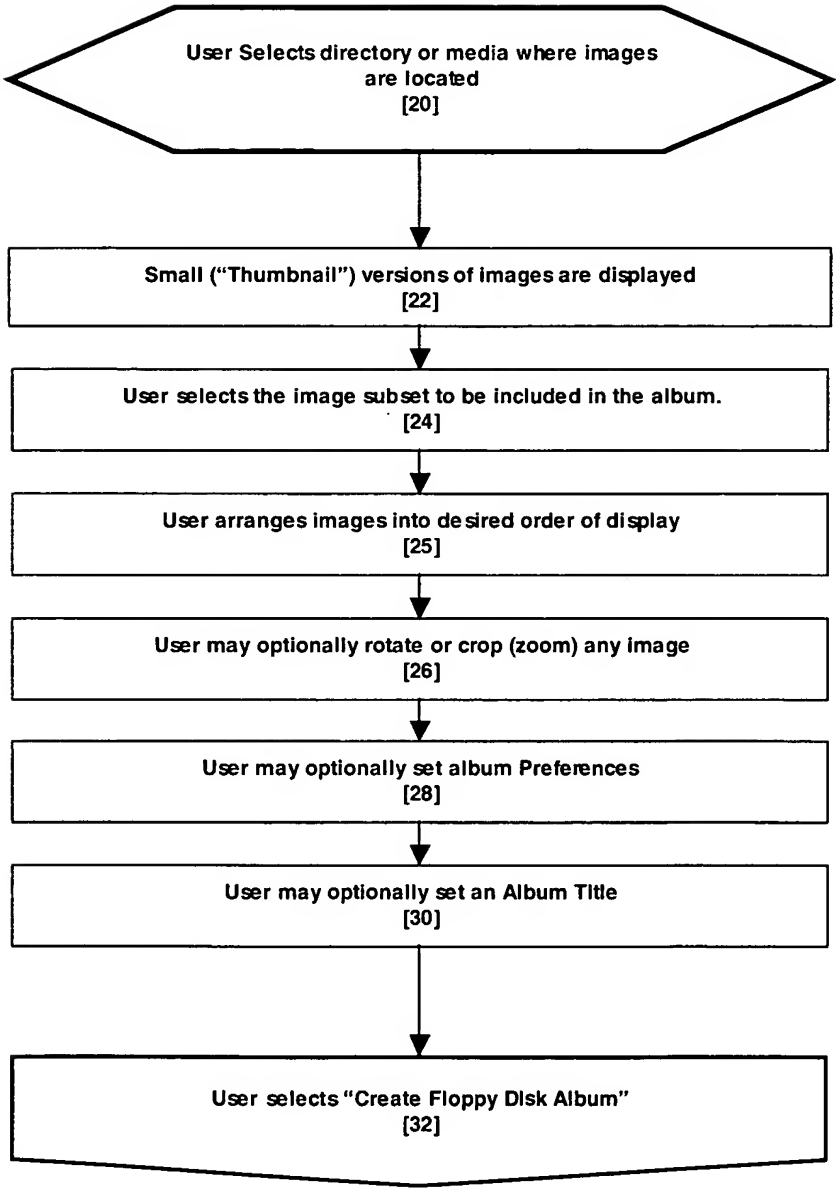
Figure 1



1005850.03202

Figure 2



LEGAL_DOCS

Figure 3

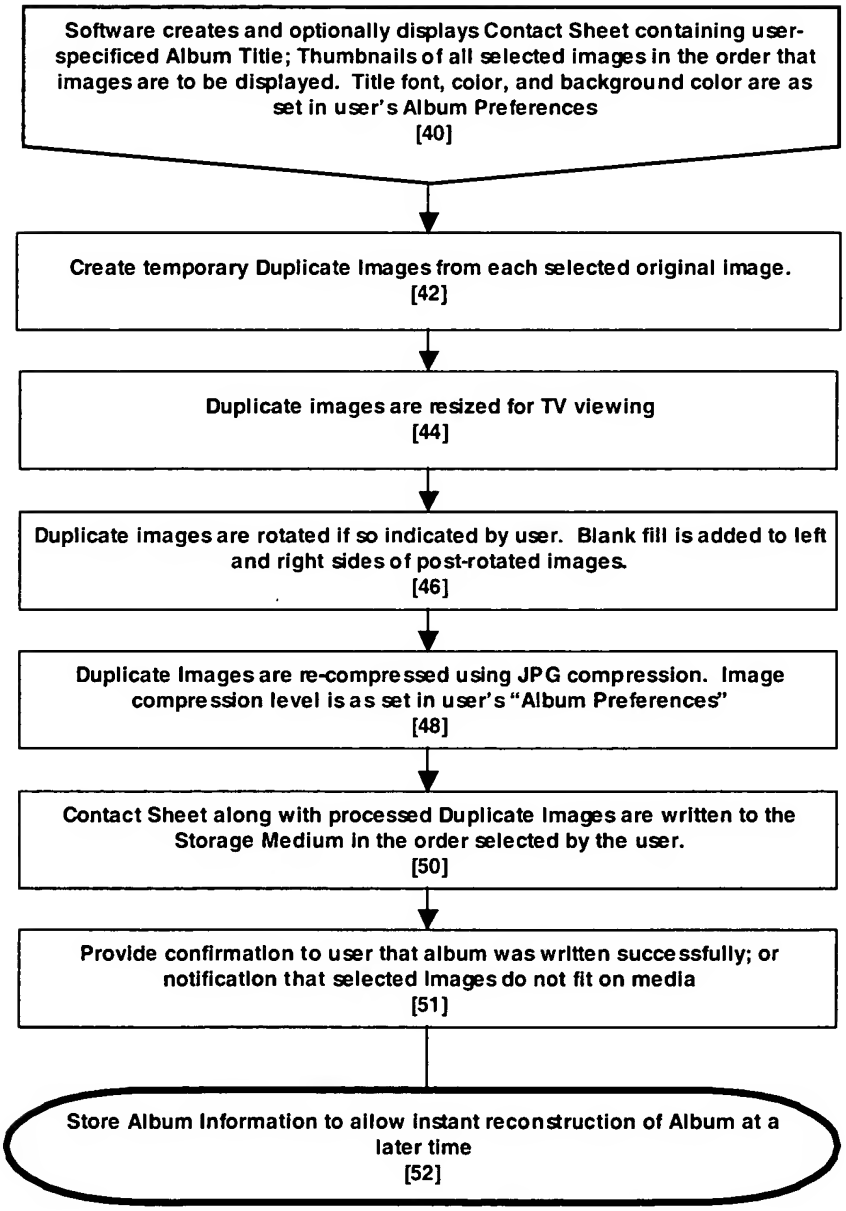

Software creates and optionally displays Contact Sheet containing user-specificed Album Title; Thumbnails of all selected images in the order that images are to be displayed. Title font, color, and background color are as set in user's Album Preferences
[40]
Create temporary Duplicate Images from each selected original image.
[42]
Duplicate images are resized for TV viewing
[44]
Duplicate images are rotated if so indicated by user. Blank fill is added to left and right sides of post-rotated images.
[46]
Duplicate Images are re-compressed using JPG compression. Image compression level is as set in user's "Album Preferences"
[48]
Contact Sheet along with processed Duplicate Images are written to the Storage Medium in the order selected by the user.
[50]
Provide confirmation to user that album was written successfully; or notification that selected Images do not fit on media
[51]
Store Album Information to allow instant reconstruction of Album at a later time
[52]

Figure 4

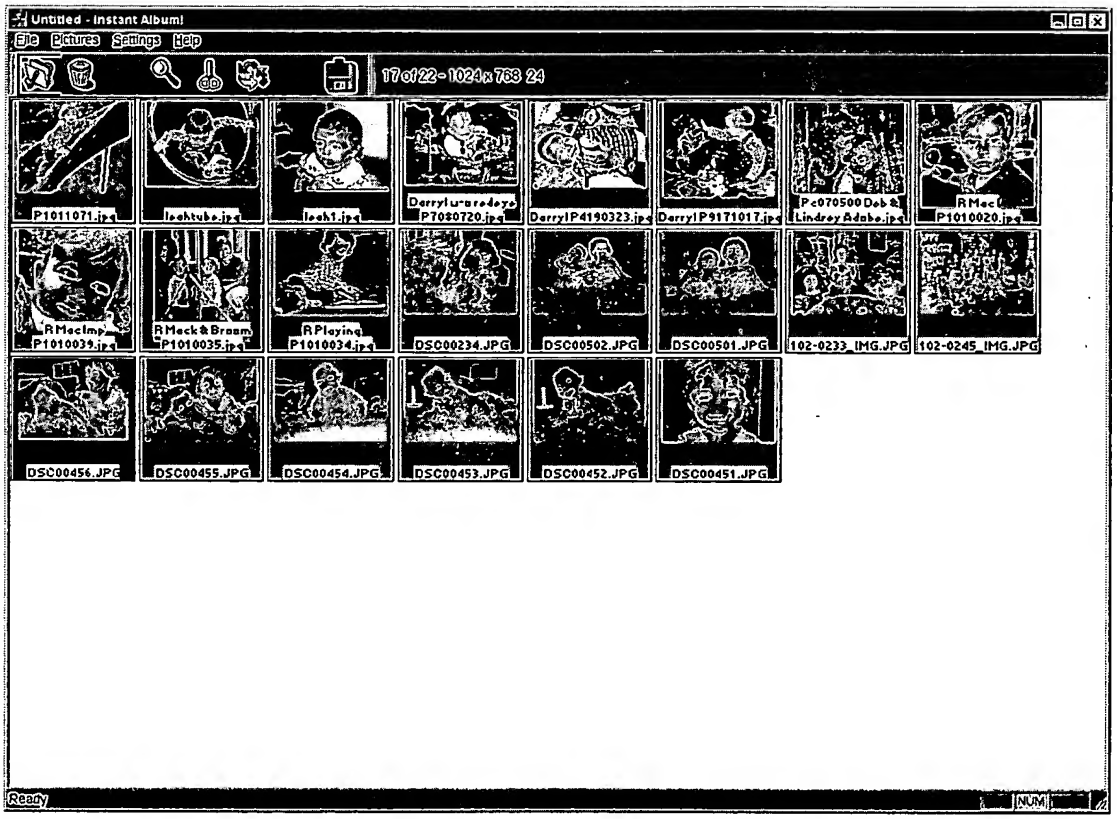
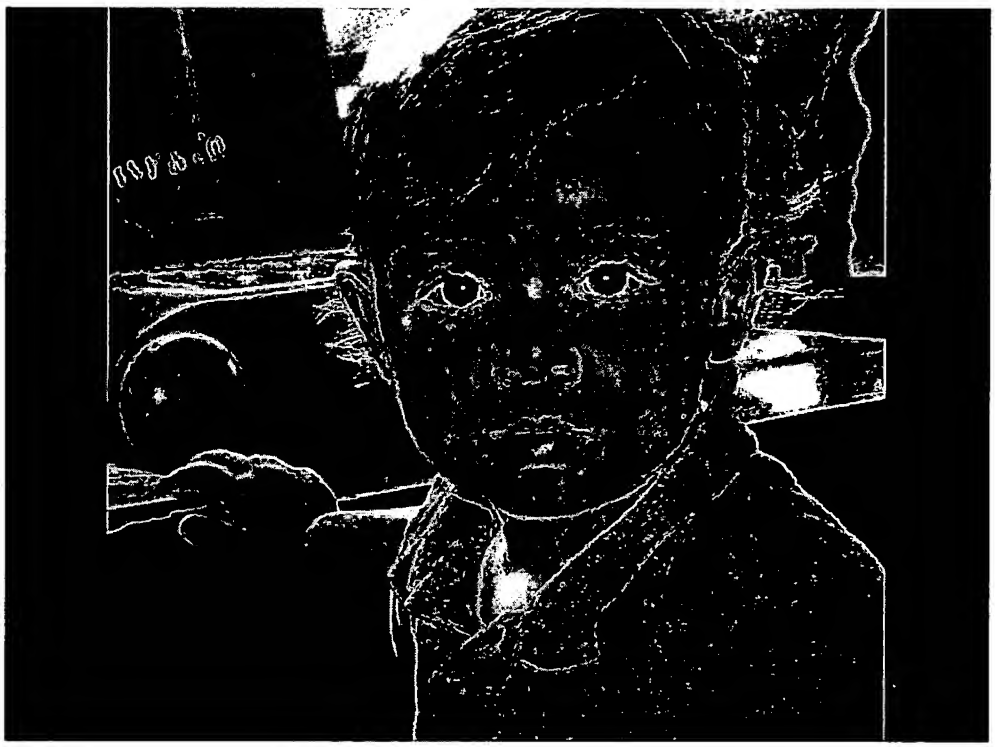

Untitled - Instant Album!
File Pictures Settings Help
17 of 22 - 1024 x 768 24
P1011071.jpg
leahtube.jpg
leah1.jpg
Darryl u-are4eyes P7080720.jpg
DarrylP4190323.jpg
DarrylP9171017.jpg
Pc070500 Deb & Lindsey Adobe.jpg
RMac P1010020.jpg
RMacImp P1010039.jpg
RMack&Braam P1010035.jpg
RPlaying P1010034.jpg
DSC00234.JPG
DSC00502.JPG
DSC00501.JPG
102-0233_IMG.JPG
102-0245_IMG.JPG
DSC00456.JPG
DSC00455.JPG
DSC00454.JPG
DSC00453.JPG
DSC00452.JPG
DSC00451.JPG
Ready
NUM

Figure 5

1005869.01200

Figure 6

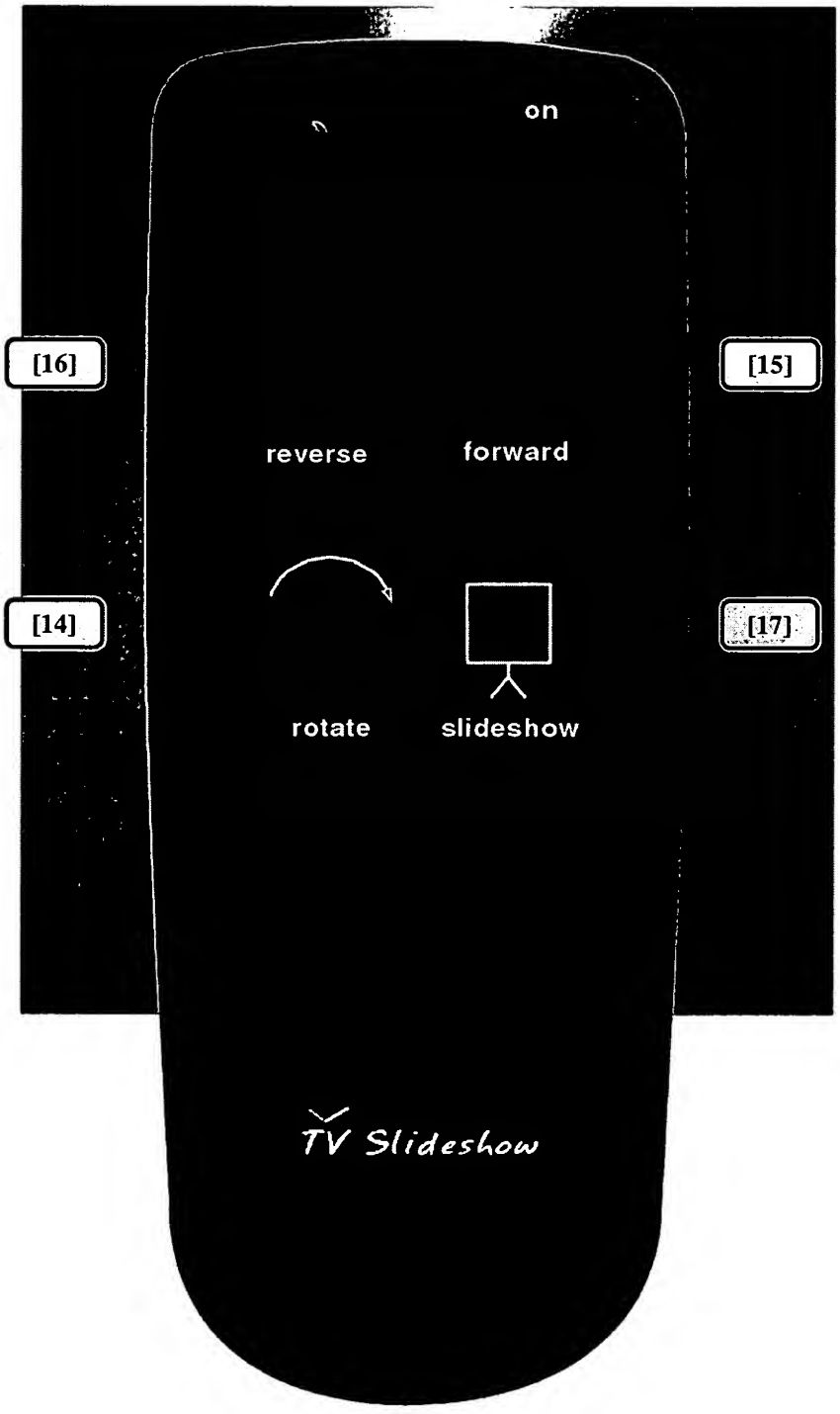


20030174.6080502

Figure 7

1005868.01

Figure 8



20050260.02600

Figure 9

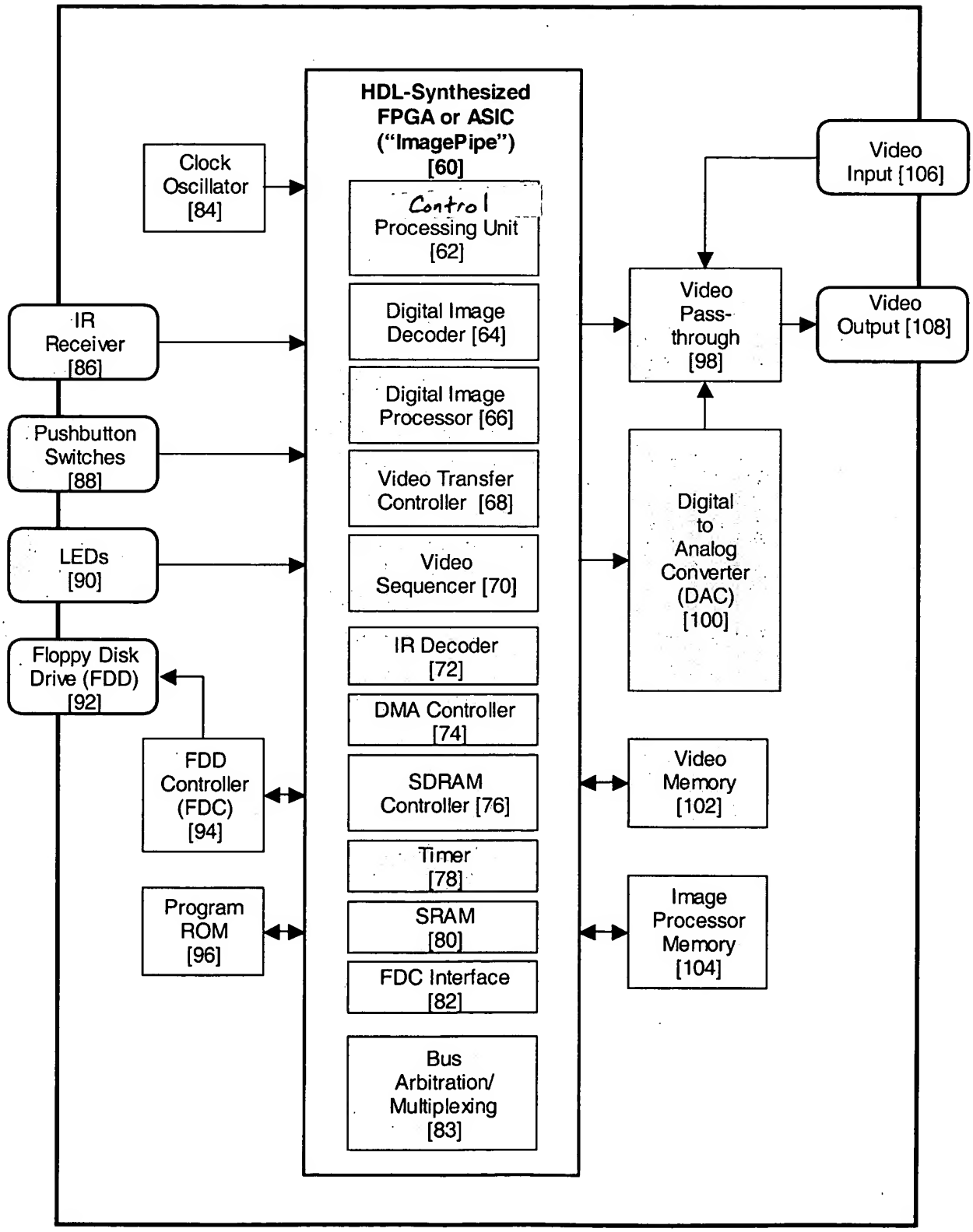

HDL-Synthesized FPGA or ASIC ("ImagePipe") [60]
Clock Oscillator [84]
IR Receiver [86]
Pushbutton Switches [88]
LEDs [90]
Floppy Disk Drive (FDD) [92]
FDD Controller (FDC) [94]
Program ROM [96]
Control Processing Unit [62]
Digital Image Decoder [64]
Digital Image Processor [66]
Video Transfer Controller [68]
Video Sequencer [70]
IR Decoder [72]
DMA Controller [74]
SDRAM Controller [76]
Timer [78]
SRAM [80]
FDC Interface [82]
Bus Arbitration/ Multiplexing [83]
Video Input [106]
Video Pass-through [98]
Video Output [108]
Digital to Analog Converter (DAC) [100]
Video Memory [102]
Image Processor Memory [104]

Figure 10

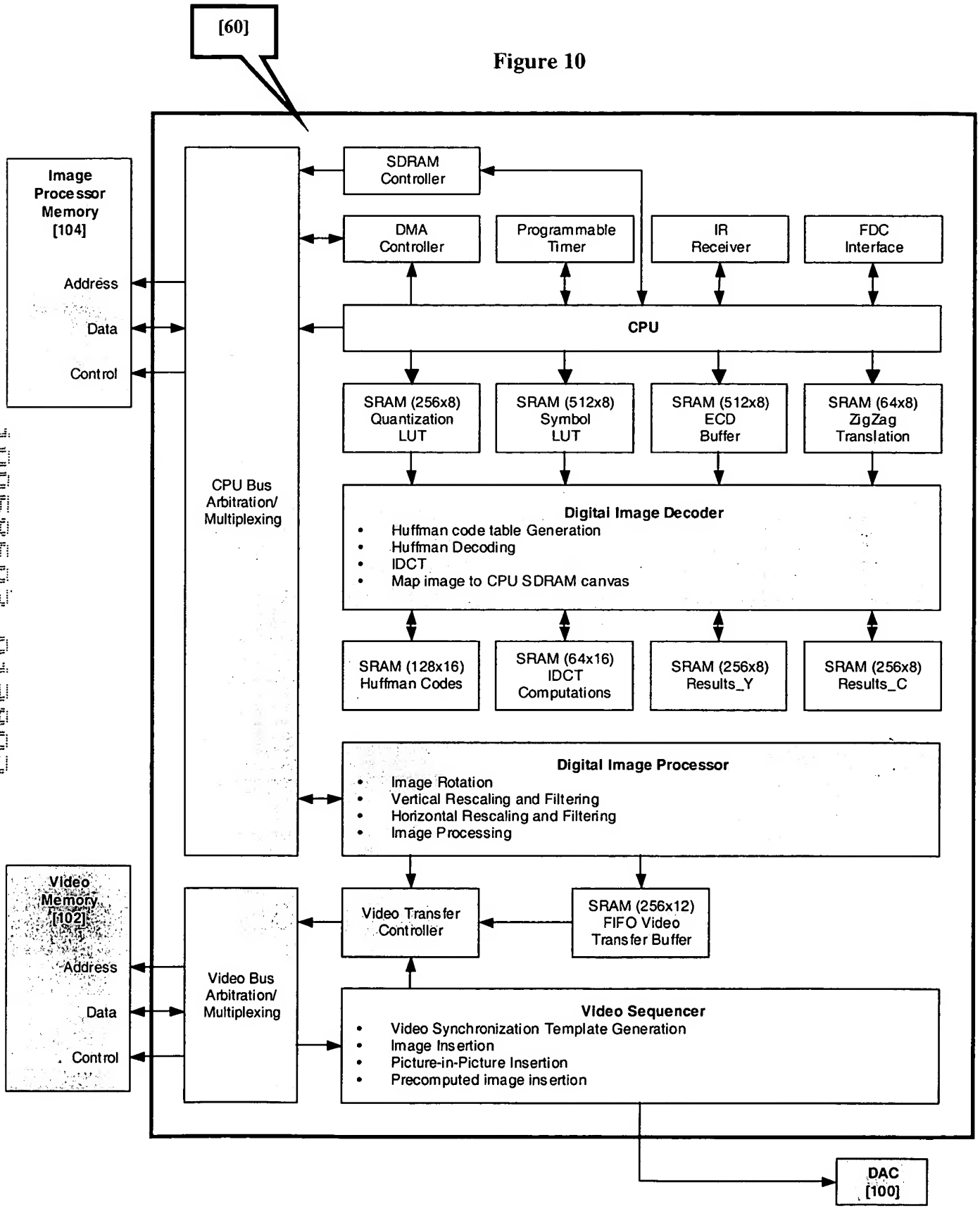
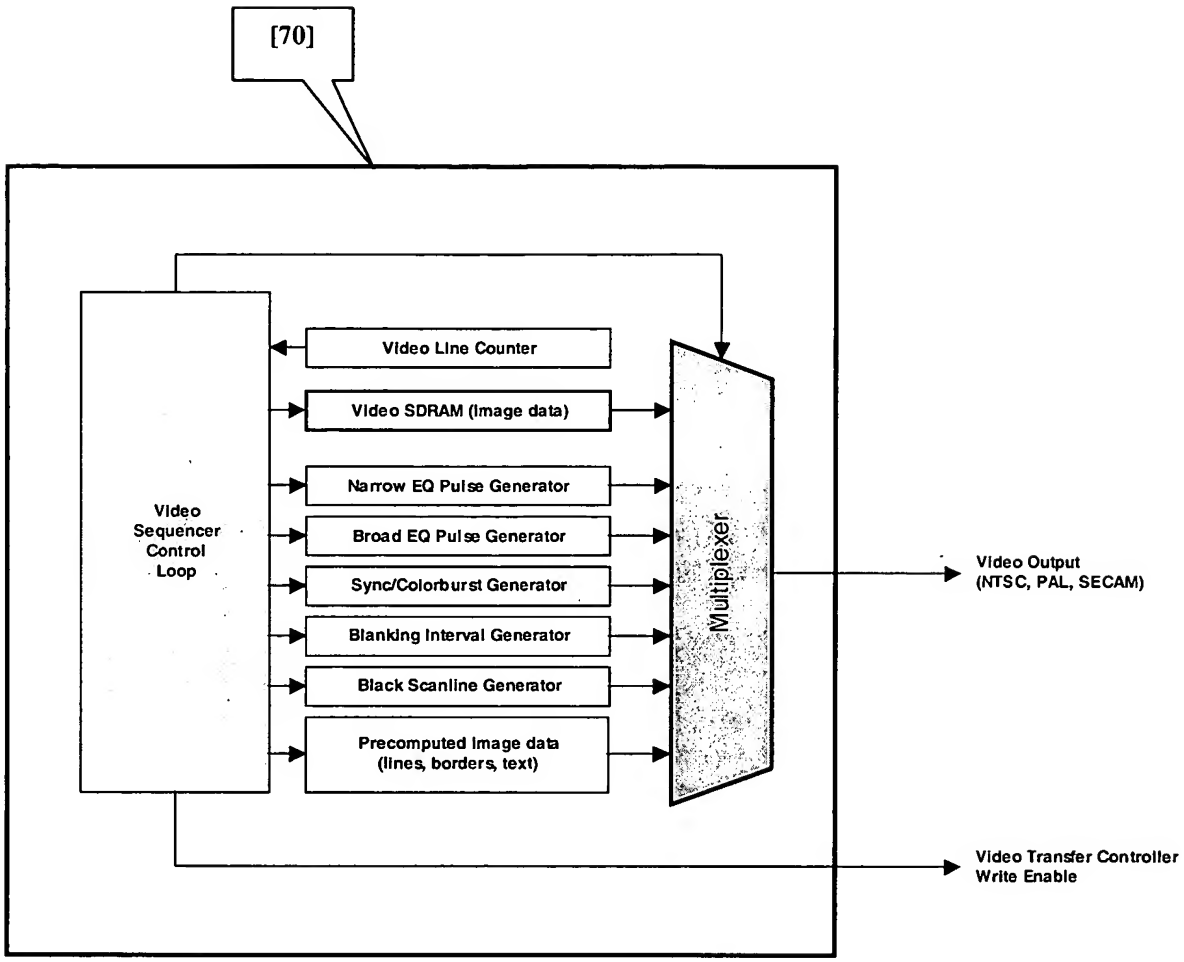

[60]
Image Processor Memory [104]
Address
Data
Control
CPU Bus Arbitration/ Multiplexing
SDRAM Controller
DMA Controller
Programmable Timer
IR Receiver
FDC Interface
CPU
SRAM (256x8) Quantization LUT
SRAM (512x8) Symbol LUT
SRAM (512x8) ECD Buffer
SRAM (64x8) ZigZag Translation
Digital Image Decoder
Huffman code table Generation
Huffman Decoding
IDCT
Map image to CPU SDRAM canvas
SRAM (128x16) Huffman Codes
SRAM (64x16) IDCT Computations
SRAM (256x8) Results_Y
SRAM (256x8) Results_C
Digital Image Processor
Image Rotation
Vertical Rescaling and Filtering
Horizontal Rescaling and Filtering
Image Processing
Video Memory [102]
Address
Data
Control
Video Bus Arbitration/ Multiplexing
Video Transfer Controller
SRAM (256x12) FIFO Video Transfer Buffer
Video Sequencer
Video Synchronization Template Generation
Image Insertion
Picture-in-Picture Insertion
Precomputed image insertion
DAC [100]

Figure 11



Patent Application

Figure 12

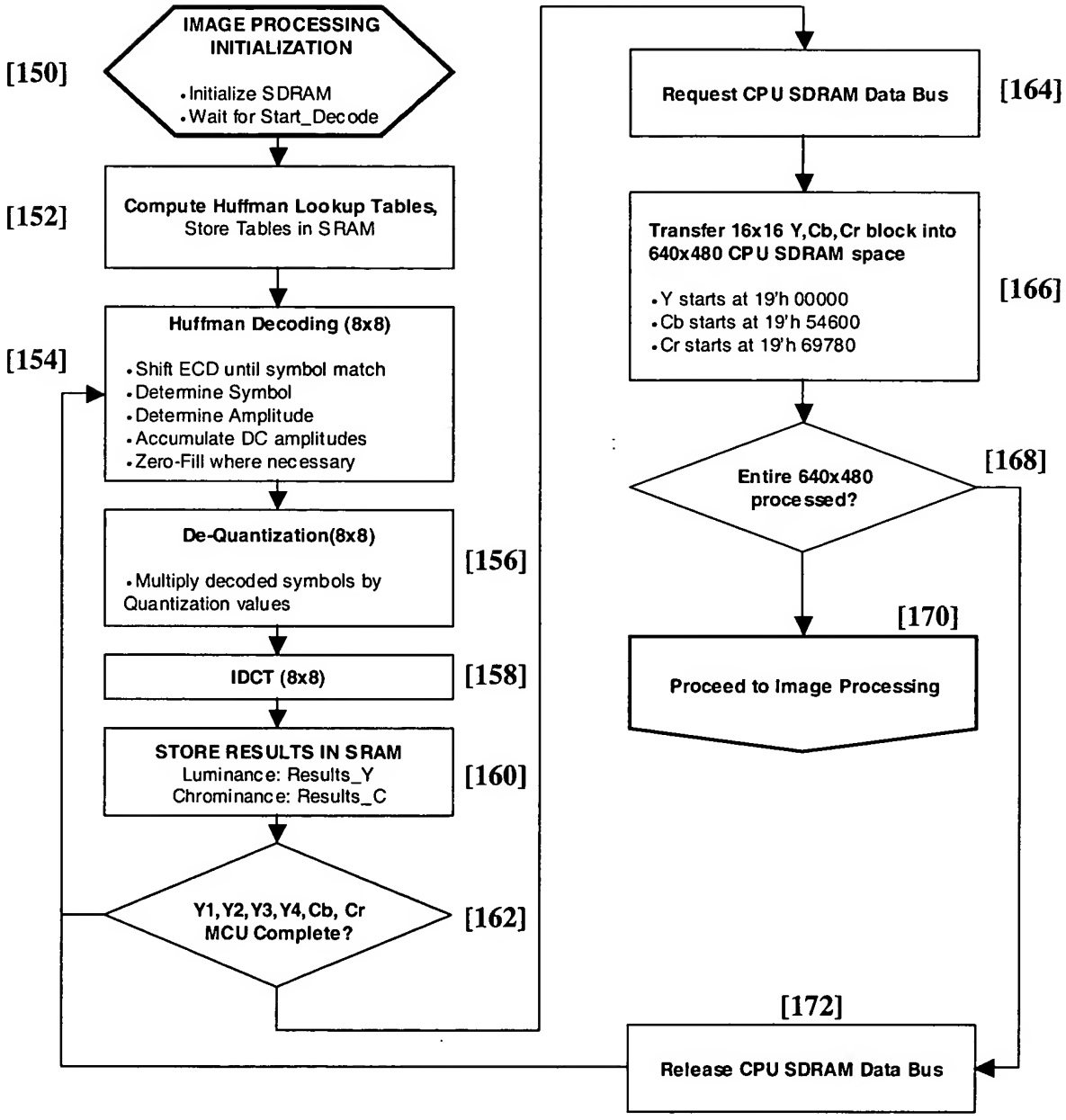


IMAGE PROCESSING INITIALIZATION
• Initialize SDRAM
• Wait for Start_Decode
[150]
Compute Huffman Lookup Tables, Store Tables in SRAM
[152]
Huffman Decoding (8x8)
• Shift ECD until symbol match
• Determine Symbol
• Determine Amplitude
• Accumulate DC amplitudes
• Zero-Fill where necessary
[154]
De-Quantization(8x8)
• Multiply decoded symbols by Quantization values
[156]
IDCT (8x8)
[158]
STORE RESULTS IN SRAM
Luminance: Results_Y
Chrominance: Results_C
[160]
Y1, Y2, Y3, Y4, Cb, Cr MCU Complete?
[162]
Request CPU SDRAM Data Bus
[164]
Transfer 16x16 Y,Cb,Cr block into 640x480 CPU SDRAM space
• Y starts at 19'h 00000
• Cb starts at 19'h 54600
• Cr starts at 19'h 69780
[166]
Entire 640x480 processed?
[168]
[170]
Proceed to Image Processing
[172]
Release CPU SDRAM Data Bus

Figure 13

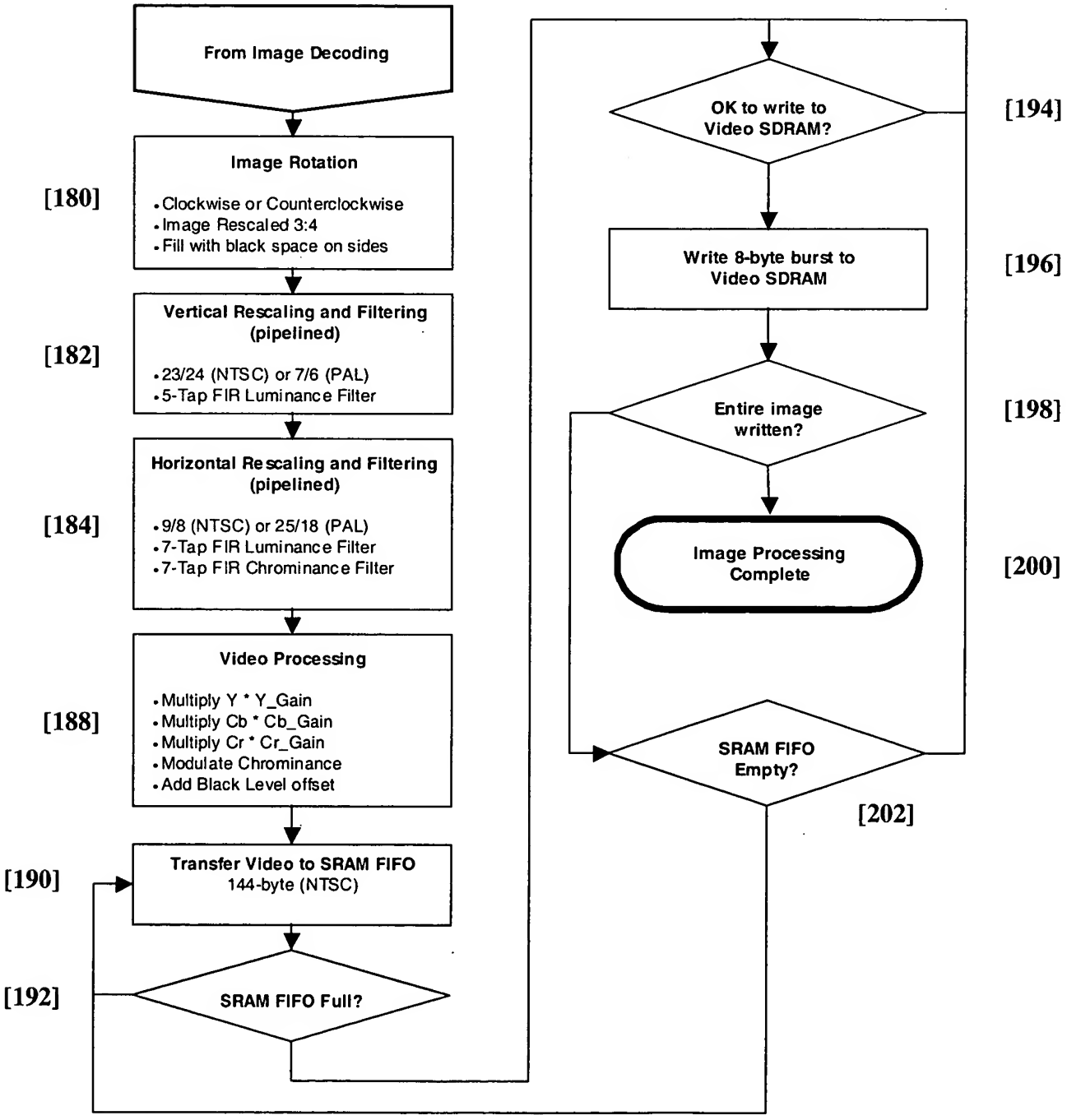
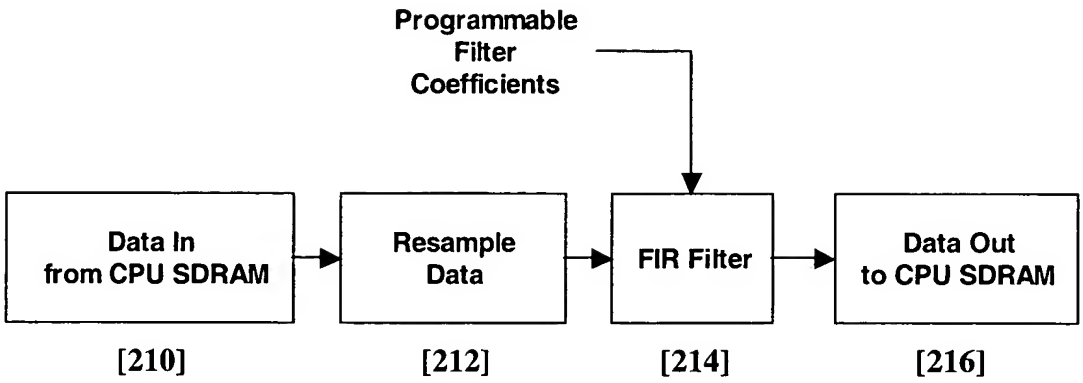

From Image Decoding
Image Rotation
• Clockwise or Counterclockwise
• Image Rescaled 3:4
• Fill with black space on sides
[180]
Vertical Rescaling and Filtering (pipelined)
• 23/24 (NTSC) or 7/6 (PAL)
• 5-Tap FIR Luminance Filter
[182]
Horizontal Rescaling and Filtering (pipelined)
• 9/8 (NTSC) or 25/18 (PAL)
• 7-Tap FIR Luminance Filter
• 7-Tap FIR Chrominance Filter
[184]
Video Processing
• Multiply Y * Y_Gain
• Multiply Cb * Cb_Gain
• Multiply Cr * Cr_Gain
• Modulate Chrominance
• Add Black Level offset
[188]
Transfer Video to SRAM FIFO
144-byte (NTSC)
[190]
SRAM FIFO Full?
[192]
OK to write to Video SDRAM?
[194]
Write 8-byte burst to Video SDRAM
[196]
Entire image written?
[198]
Image Processing Complete
[200]
SRAM FIFO Empty?
[202]

Figure 14



EXPRESS MAIL NO. EV 405060943 US

Figure 15

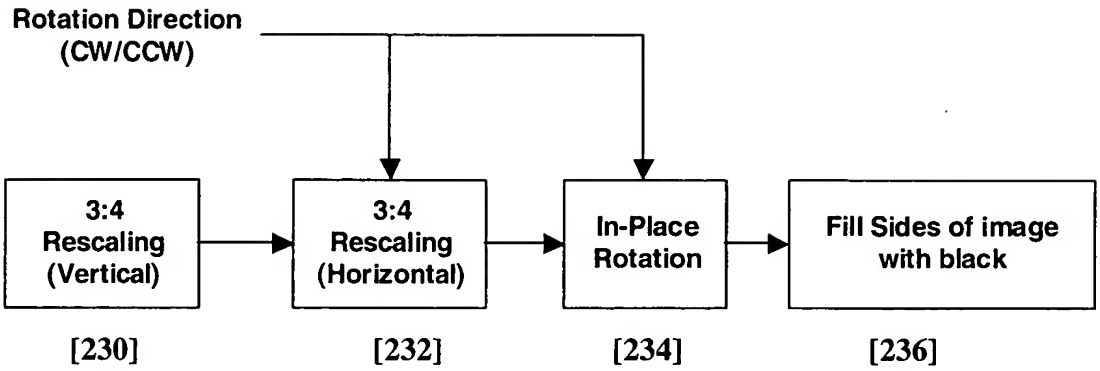
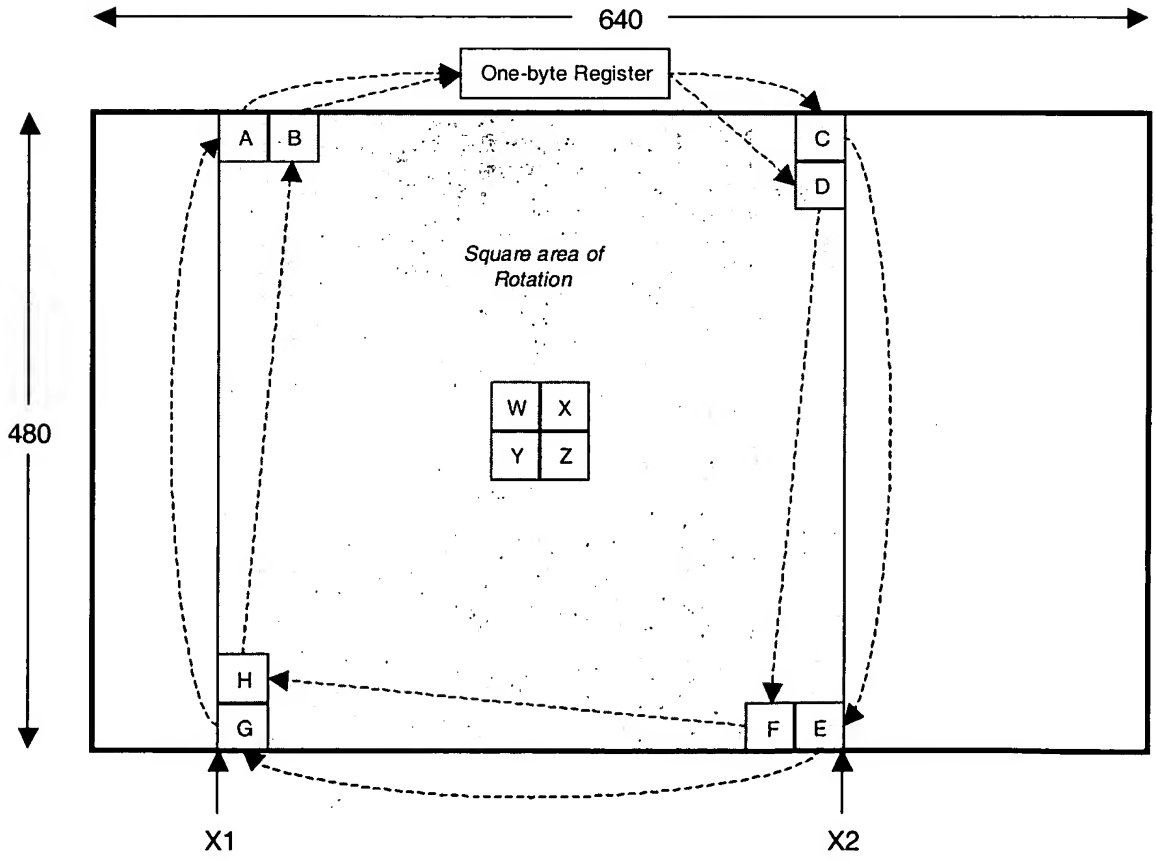



Figure 16